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Fast Charge Pump Phase Locked Loop with a BBFC: A Numerical Confirmation

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Abstract. Speeding up a synthesizer's locking process can be considered as speeding up the charge pump PLL. Several methods have been introduced to increase the speed of the locking process. One way to achieve fast locking is to use a bang-bang frequency comparator (BBFC) in the feed-trough path to achieve a faster locking process. In this paper, we present a differential equation for this fast CPPLL which shows how the BBFC can decrease the settling time in a charge pump PLL. Simulations in MATLAB are confirmed by a differential equation solved in Maple using a numerical method. Using the extracted equation and solving it by numerical method we can predict the system's behavior.

Key-Words: *BBFC, CPPLL, differential equation, fast locking, numerical solution*

1. Introduction

A local frequency generated by a frequency synthesizer is mixed with the incoming RF signal in a receiver to create a lower frequency signal that can be processed in a baseband IC. Switching between the transmit and receive frequencies has to be performed rapidly with respect to the settling time requirements of the communications standard [1]. Speeding up the synthesizer's locking process can be considered equivalent to speeding up the charge pump PLL (CPPLL) [2]. In [2] the authors presented an auxiliary bang-bang frequency comparator circuit which leads to faster locking in a traditional CPPLL. In this paper, we present a differential equation which can describe this fast process, and present the numerical results which validates the obtained equation.

The paper is organized as follows. In Sec 2, we discuss the traditional CPPLL and the fast structure on which the equations are written. In Sec 3, we present a differential equation which describes the system. In Sec 4 we compare the Matlab Simulink results with those obtained from numerical solution of the presented equation. The results are summarized in Sec 5.

2. Background

2.1. Conventional CPPLL

Fig.1 shows a traditional CPPLL in which frequency acquisition occurs effectively through charging the relatively large LF capacitor C1 to the DC value that corresponds to the control voltage of the VCO that is required to minimize the frequency error at the PFD input [3].

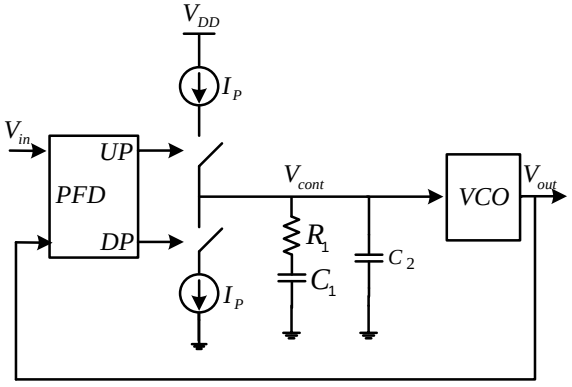


Fig. 1. The conventional Charge Pump PLL (CPPLL)

Locking transient of the traditional CPPLL shown in Fig. 2.

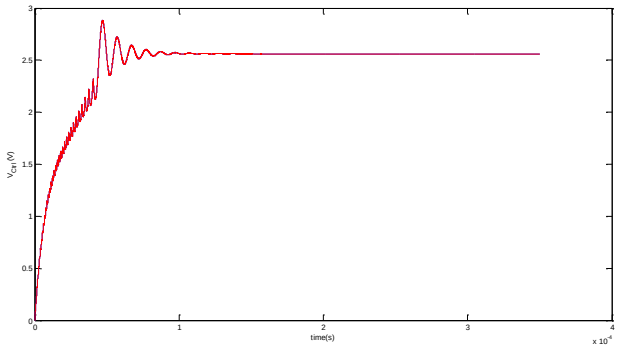


Fig. 2. Vctrl of a traditional CPPLL in response to a step input

3. A Fast Charge Pump PLL Using a Bang-Bang Frequency Comparator

In [2], we proposed a variant of [4], where the frequency comparator has a bang-bang characteristic. Its output corresponds to the sign of the frequency difference. The CPPLL with the auxiliary bang-bang frequency correction charge pump is shown in Fig. 3. The nonlinear stage is much shorter in the case of the BBFC while the linear stages of the transient are similar.

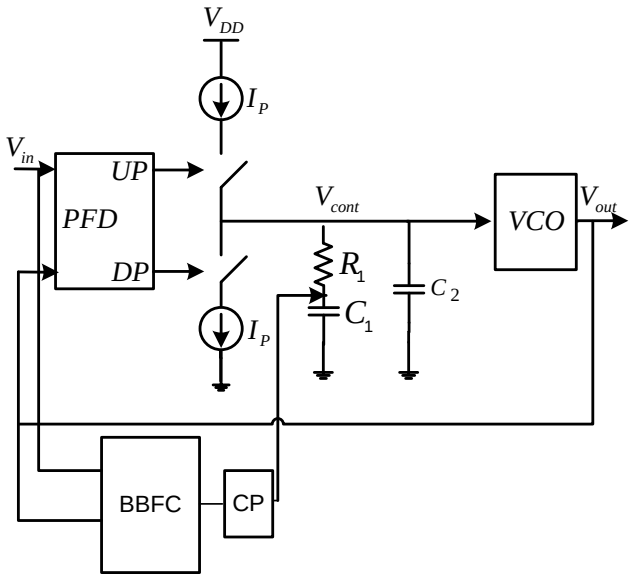


Fig. 3. Block diagram of the CPPLL with BBFC.

Fig. 1 shows a block diagram of a fast charge pump PLL. It comprises a reference oscillator, a Phase-Frequency Detector (PFD), a Charge Pump (CP), a loop filter (LPF), a Voltage-Controlled Oscillator (VCO) and an auxiliary circuit including a BBFC block. The transfer characteristic of the used BBFC is shown in Fig. 4.

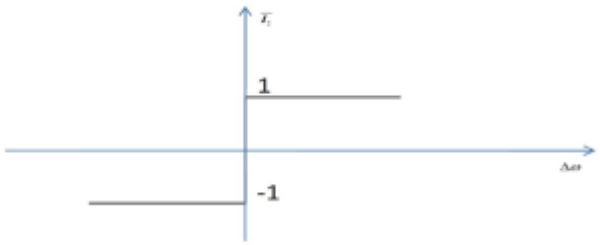


Fig. 4. Transfer characteristic of BBFC

The simulation results for a frequency step at the reference input are shown in Fig. 5. The simulation shows that the structure shown in Fig. 1 responds significantly faster than the traditional one that doesn't have the auxiliary circuit.

Matlab simulation results for a frequency step at the reference input are shown in Fig. 5. The simulation shows that the structure shown in Fig. 3 responds significantly faster than the traditional one primarily because the (nonlinear) frequency acquisition phase is shorter. In the remainder of the paper, we present an equation to see the effect of the auxiliary circuit mathematically.

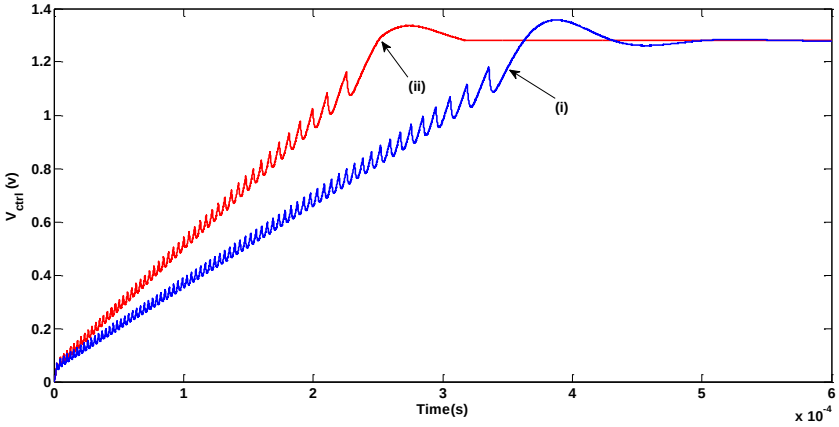


Fig. 5. Vctrl in (i) traditional, and (ii) BBFC PLLs

4. The differential equation describing the system

Considering v_{ctrl} as a criterion in Fig. 3, we write:

$$\phi_i(t) = (\omega_c + \Delta\omega)t, \tag{1}$$

Where ω_c is the input frequency, and $\Delta\omega$ is the applied frequency step. The VCO is governed by an affine model:

$$\phi_o(t) = \omega_c t + K_{VCO}\int_0^t V_{ctrl}(t)dt, \tag{2}$$

Where V_{ctrl} is the control voltage applied to its input. Equivalently:

$$\phi_o'(t) = \omega_c + K_{VCO}V_{ctrl}(t), \tag{3}$$

On the other side, we have:

$$I_1 = K_{PD}(\phi_i(t) - \phi_o(t)), \tag{4}$$

Where K_{PD} is the transfer gain from the input of the PFD to the output of the charge pump that is equal to $\frac{I_P}{2\pi}$ [3]. Therefore,

$$I_1' = K_{PD}(\phi_i'(t) - \phi_o'(t)) = K_{PD}(\omega_c + \Delta\omega - \omega_c - K_{VCO}V_{ctrl}(t)), \tag{5}$$

hence,

$$\boldsymbol{I_1'} = \boldsymbol{K_{PD}}(\Delta\omega - \boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}'}(\boldsymbol{t})), \tag{6}$$

hence,

$$\boldsymbol{V_{ctrl}} = \boldsymbol{I_1}\boldsymbol{R_1} + \frac{1}{\boldsymbol{C_1}}\int_0^{\boldsymbol{t}}(\boldsymbol{I_1} + \boldsymbol{I_2})\boldsymbol{dt}, \tag{7}$$

therefore,

$$\boldsymbol{I_2} = \boldsymbol{K_{BB}}\boldsymbol{sign}(\boldsymbol{\phi_i'}(\boldsymbol{t}) - \boldsymbol{\phi_o'}(\boldsymbol{t})) = \boldsymbol{K_{BB}}\boldsymbol{sign}(\omega_c + \Delta\omega - \omega_c - \boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}}(\boldsymbol{t})), \tag{8}$$

By derivation of (7)

$$\boldsymbol{V_{ctrl}'} = \boldsymbol{I_1'}\boldsymbol{R_1} + \frac{1}{\boldsymbol{C_1}}(\boldsymbol{I_1} + \boldsymbol{I_2}), \tag{9}$$

Therefore,

$$\begin{aligned}\boldsymbol{V_{ctrl}'} &= \boldsymbol{K_{PD}}(\omega_c + \Delta\omega - \omega_c - \boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}}(\boldsymbol{t}))\boldsymbol{R_1} \\ &+ \frac{1}{\boldsymbol{C_1}}(\boldsymbol{K_{PD}}(\boldsymbol{\phi_i}(\boldsymbol{t}) - \boldsymbol{\phi_o}(\boldsymbol{t})) + \boldsymbol{K_{BB}}\boldsymbol{sign}(\boldsymbol{\phi_i'}(\boldsymbol{t}) - \boldsymbol{\phi_o'}(\boldsymbol{t})))\end{aligned} \tag{10}$$

And finally,

$$\begin{aligned}\boldsymbol{V_{ctrl}''} &= \boldsymbol{K_{PD}}(-\boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}'}(\boldsymbol{t}))\boldsymbol{R_1} + \frac{1}{\boldsymbol{C_1}}\boldsymbol{K_{PD}}((\Delta\omega - \boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}'}(\boldsymbol{t})) \\ &+ 2\boldsymbol{K_{BB}}\boldsymbol{sign}(-\boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}'}(\boldsymbol{t}))\delta(\Delta\omega - \boldsymbol{K_{VCO}}\boldsymbol{V_{ctrl}}(\boldsymbol{t})))\end{aligned} \tag{11}$$

5. Comparison between simulations and the presented equation

5.1. Matlab simulations

To verify the effect of the auxiliary circuit in fast locking, we consider three different values for I_{BB}.
The values of the parameters used in the simulation are summarized in Table 1.

Table 1. Parameters used in the simulations

Parameter	Value
f_{PD}	256 MHz
$\Delta\omega$	0.256 MHz
R_1	0.75 kΩ
C_1	35 nf
I_P	0.15 mA
K_{VCO}	100 kHz/V
I_{BB}	0, 0.5 I_P , I_P

Fig. 6 shows the v_{ctrl} in these three cases.

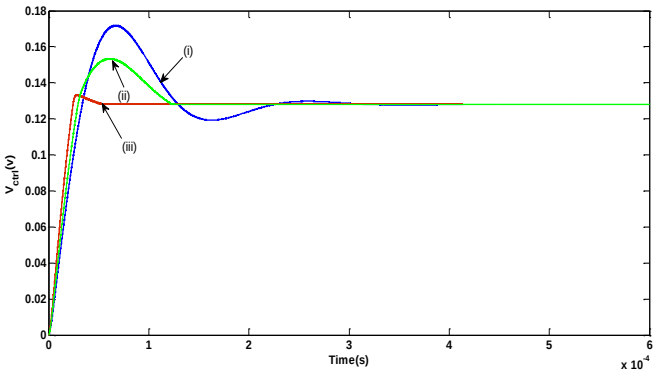


Fig. 6. Matlab Simulink results for vctrl in three different cases (i) I_{BB} = 0, (ii) I_{BB} = 0.5Ip, and (iii) I_{BB} = Ip

As we expected, the larger I_{BB}, the faster locking is achieved. Where I_{BB}=0, the circuit works as a traditional CPPLL.

5.2. Numerical solution

In this section, we need to solve Eq. 11; because of inherent properties of Eq. 11, it is inferred that this equation doesn't have an explicit solution.

Consequently, we solve it using numerical methods. Considering runge-kutta method in Maple [5], the curves shown in Fig.7 are obtained. For more consistency, the parameters used in the numerical solution are the same as the parameters used in the previous section as listed in Table I.

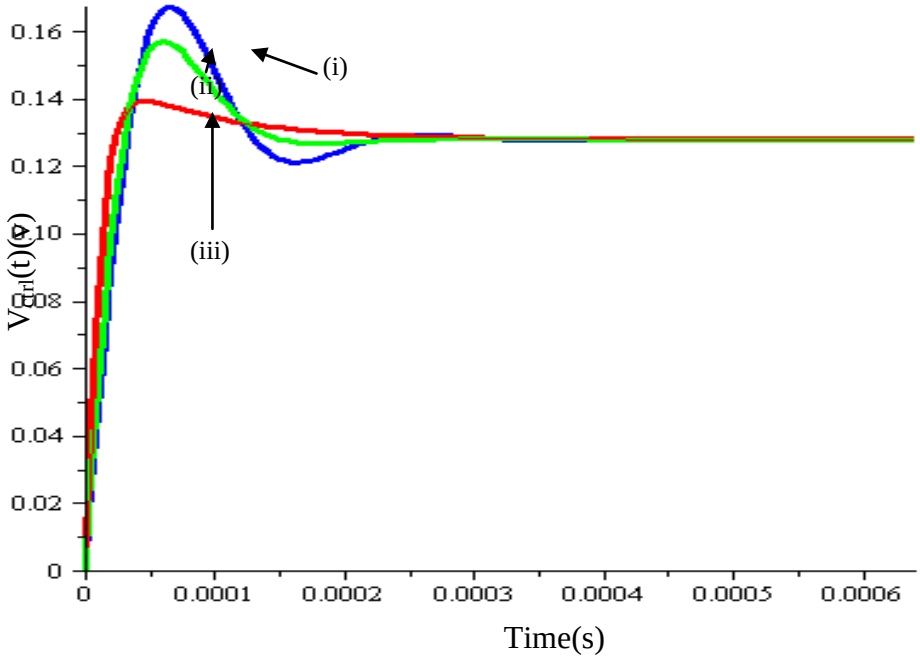


Fig. 7. Numerical solution for v_{ctrl} in three different cases (i) IBB = 0, (ii) IBB = 0.5Ip, and (iii) IBB = Ip

From Fig. 5, the effect of the IBB in faster locking is verified. Furthermore, by comparing Fig. 4 and Fig. 5, one can infer that the presented equation has a proper accuracy and as a result, it can be used to predict the behavior of the fast lock CPPLL with the BBFC. In particular, it is also capable of predicting the transient of a CPPLL where I_{BB}=0;

6. Conclusions

In this paper we have described a differential equation for the v_{ctrl} in a fast locking charge pump PLL which uses an auxiliary bang-bang frequency comparator as a lock-aid circuit. We have solved the presented equation using numerical methods. Considering the obtained results, both the efficiency of the BBFC to achieve faster locking, and proper accuracy of the suggested equation are verified.

Appendix

Solving the equation in Maple

Considering (Eq. 10 or 11), one can notice that because of the presence of *the sign* and its derivative, solving the equations are complex. The easiest way to overcome the problem is to replace *the sign (.)* function which is not differentiable at 0 with a differentiable function whose derivative exists at each point in its domain. Hence, we used *tanh (.)* which has similar features to *sign (.)* especially when it is far from the origin i.e. when the system is out of luck. Considering the applied frequency step, we used *tanh (.)* instead of *sign (.)* which has suitable transfer characteristics as shown in Fig. 8. The code used in Maple to obtain the numerical results for K_{BB}=0 is shown in Fig.9

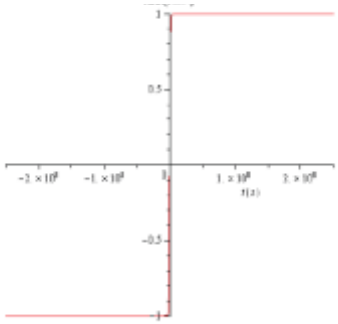
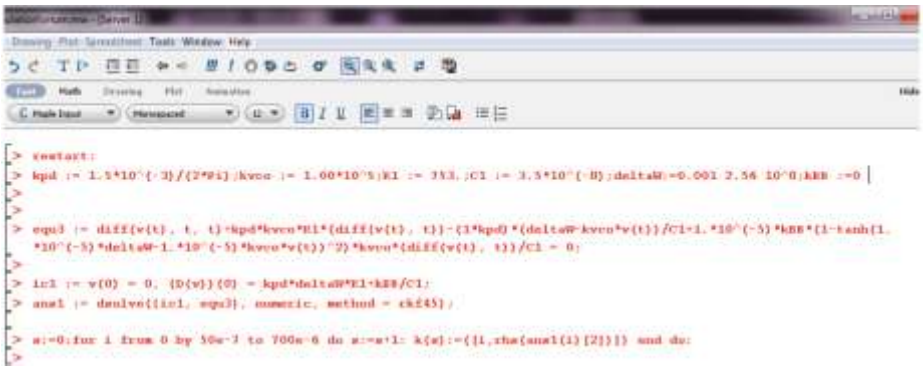


Fig. 8. The characteristic of *tanh (.)* which we used to solve the equation



```
> restart:
> kpd := 1.5*10^(-3)/(2*Pi):kvco := 1.00*10^5:K1 := 353.:C1 := 3.5*10^(-8):deltaW:=0.001 2.56 10^0:kBB :=0
>
>
> eqn3 := diff(v(t), t, t)+kpd*kvco*K1*(diff(v(t), t))-(1*kpd)*(deltaW-kvco*v(t))/C1+1.*10^(-5)*kBB*(1-tanh(1.
  *10^(-5)*deltaW-1.*10^(-5)*kvco*v(t))^2)*kvco*(diff(v(t), t))/C1 = 0;
>
> ic1 := v(0) = 0, (D(v))(0) = kpd*deltaW*K1*kBB/C1:
> ans1 := dsolve({ic1, eqn3}, numeric, method = rkf45):
>
> a:=0:for i from 0 by 50e-3 to 700e-6 do a:=a+1: k[a]:=([1,rhs(ans1(1)[2])]) end do:
>
```

Fig. 9. A typical Maple code used for solving the presented differential equation

References

[1] V. Valenta, M. Villegas, and G. Baudoin, "Analysis of a PLL Based Frequency Synthesizer using Switched Loop Bandwidth for Mobile WiMAX."

[2] V. S. Sadeghi, and H. M. Naimi, "A Fast Synthesizer Using a Bang-Bang Frequency Comparator and Locking Status Indicator," in International Conference on Electrical Engineering and Informatics (ICEEI2011), Bandung, Indonesia, 2011, pp. 1-4.

[3] B. Razavi, *Design Of Analog CMOS Integrated Circuits* p.^pp. 532-578: Mc Grow Hill, 2001.

[4] S. Liu, and Y. Shi, "Fast Locking and High Accurate Current Matching Phase-Locked Loop," 2008.

[5] L. F. Shampine, and R.M.Corless, "Initial Value Problems for ODEs in Problem Solving Environments," *Comp. Appl. Math*, vol. 125, no. 1-2, pp. 31-40, 2000.